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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,972	09/26/2003	Masakatsu Uneme	N28733102E	3617

7590 02/06/2006

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EXAMINER	
TSAI, SHENG JEN	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/672,972	Applicant(s) UNEME, MASAKATSU	
	Examiner Sheng-Jen Tsai	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Remarks filed on January 9, 2006 regarding application 10,672,972 filed on September 26, 2003.

2. Claims 1-21 are pending in the application under consideration.

3. ***Response to Remarks***

Applicant's remarks have been fully and carefully considered with the Examiner's response set forth below.

Response to remark on 112, second paragraph rejections

Rejections of claims 2 and 20 under 35 U.S.C 112, second paragraph have been withdrawn. The interpretation of the term "linearly aligned" will be according to the illustrations of figures 3 and 7 of the Application.

Response to remark on claim 1

Applicant contends that Yanagawa (US Patent Application Publication 2001/0046163) does not teach the limitation of "**wherein each m output circuit is physically adjacent to a corresponding one of the m data output terminals**," as recited in claim 1. The Examiner disagrees with this assessment for the following reason.

First, Figure 2 of Yanagawa shows a 32-bit DATA connection port between the memory device (figure 2, 11) and the memory controller (figure 2, 10). Since the 32-bit DATA port serves as the connection port between the two devices, it is inherent that there are 32-bit terminals at each side of the device so that connection can be made. Since the 32-bit connection port is a bi-directional data port, as shown in figure 2, the

corresponding 32-bit terminal at each side of the device serves as both input and output terminal.

Second, Figure 2 of Yanagawa shows that the only entity between the 32-bit DATA connection port and the 32-bit DATA output signals is an INTERFACE unit (figure 2, 24). In other words, the 32-bit DATA output terminals are physically located at the left-hand side of the INTERFACE unit and the 32-DATA output signals are physically located at the right-hand side of the INTERFACE unit, as clearly shown in figure 2. Thus, it is clear that the 32-bit DATA output signal is physically most adjacent to the 32-bit DATA connection port than any other elements of the memory controller (figure 2, 10). Their physical proximity is clearly illustrated in figure 2.

Third, According to IEEE 100, The Authoritative Dictionary of IEEE Standards Terms (7th edition, IEEE Press, 2000, ISBN 0-7381-2601-2, page 574), the definition of an interface for data transmission is "a common boundary; for example, a physical connection between two systems or two devices. The boundary may be mechanical such as the physical surfaces and spacing in mating parts, modules, components, or subsystems, or electrical, such as matching signal levels, impedances, or power levels." Since the INTERFACE unit is internal to the memory controller, and both the 32-bit DATA output signals and the 32-bit DATA terminals are both electrical in nature, one of ordinary skills in the art would understand that the INTERFACE unit may be as simple as direct wiring, or at most of signal conditioning (signal level, impedance) to match different type of technologies (TTL, COMS) if necessary. Either way, their physical adjacency is evident by being at the two ends of an INTERFACE unit.

Therefore, the Examiner's position regarding claim 1, and those claims dependent from it, remains the same as stated in the previous Office Action.

<u>Response to remark on claims 8 and 14</u>

Applicant contends that Yanagawa (US Patent Application Publication 2001/0046163) does not teach the limitation of "**first and second wiring corresponding to each input holding circuit being <u>essentially</u> equal in length**," and "**the length of the first wiring to each second latch circuit is <u>essentially</u> equal to the sum of the lengths of the second and third wirings**," as recited in claims 8 and 14, respectively. The Examiner disagrees with this assessment for the following reason.

Yanagawa teaches that "even when the delay of the variable delay circuits varies due to <u>a variety of variation factors</u> such as variation of the manufacturing process, variation in ambient temperature, and variation in the power supply voltage, proper delay control based on the phase comparison of clock signals <u>makes it possible to adjust the delay of the variable delay circuit 51-5 to be equal to the 1/4 cycle of the clock signal</u>. Under the conditions in which a variety of variation factors are present, therefore, optimum data acquisition timing can be achieved" (paragraph 0064).

Since it is possible to adjust the delay of the variable delay circuit to be equal to the ¼ cycle of the clock signal, the wirings, or signal paths, are <u>essentially</u> equal <u>electrically</u> for the purpose of signal synchronization.

Therefore, the Examiner's position regarding claims 8 and 14 remains the same as stated in the previous Office Action.

Response to remark on claims 15-19

Applicant again contends that Yanagawa (US Patent Application Publication 2001/0046163) does not teach the limitation of "**essentially equal in length**," as recited in the claims.

This issue has been addressed earlier. Refer to "Response to remark on claims 8 and 14."

Therefore, the Examiner's position regarding claims 15-19 remains the same as stated in the previous Office Action.

Response to remark on claims 3-4 and 6

Applicant again contends that Yanagawa (US Patent Application Publication 2001/0046163) does not teach the limitation of "**each m output circuit is physically adjacent to a corresponding one of the m data output terminals**," as recited in the claims.

This issue has been addressed earlier. Refer to "Response to remark on claim 1."

Therefore, the Examiner's position regarding claims 3-4 and 6 remains the same as stated in the previous Office Action.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2, 5, and 7-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Yanagawa (US Patent Application Publication 2001/0046163).

As to claim 1, Yanagawa discloses **a memory controller** [figure 1, 10] **connected to a semiconductor memory device** [figure 1, 11], **comprising**:

a clock generating circuit that generates an output clock signal [figure 2, 21];

a data generating circuit that provides output digital data [figure 2, 32 bits DATA into the interface (24) and 32 bits DATA from the interface];

a predetermined number "m" data output terminals that provide output data to the semiconductor memory device in parallel [figure 2, 32 bits DATA to and from the memory device, m=32];

m output holding circuits for storing the output digital data synchronously with the output clock signal [32 bits latch circuits (figure 2, 30, 31 and 27)];

a predetermined number "n" signal output terminals that provide output strobe signals to the semiconductor memory device in synchronism with the output data, where n<m [strobe signals, figure 2; figure 12; figures 13A and 13B; figure 15; n=1]; **and**

a plurality of output delay circuits including one output delay circuit for every "p" signal output terminal(s), where p is an integer greater than zero, each output delay circuit delaying the output clock signal by a predetermined amount to transmit an output strobe signal to the corresponding p signal output terminal(s) [figure 3 shows a plurality of delay circuits; figures 8-11; figure 15; figure

25; p=1 as a delay circuit is associated with each strobe signal; a data acquisition circuit which delays the strobe signal (abstract); paragraph 0025];

wherein each m output holding circuit is physically adjacent to a corresponding one of the m data output terminals [figures 2, 5-7; refer to "Response to remark on claim 1"]; **and**

the output of each output delay circuit is adjacent to the corresponding p signal output terminal(s) [figures 2, 5-7; refer to "Response to remark on claim 1"].

As to claim 2, Yanagawa teaches that **the m output data output terminals and n signal output terminals are linearly aligned with one another** [figure 2 shows that the 32-bit DATA output terminals are physically located at the left-hand side of the INTERFACE unit and the 32-DATA output signals are physically located at the right-hand side of the INTERFACE unit, and there is a one-to-one correspondence between the two groups of 32-bit DATA signals. Note that this is consistent with the illustrations of figures 3 and 7 of the Application]; **the m holding circuits are linearly aligned with one another** [figure 25; Note that this is consistent with the illustrations of figures 3 and 7 of the Application]; and the plurality of output delay circuits are linearly aligned with one another between m holding circuits and the aligned m data output terminals and n signal output terminals [figure 25; Note that this is consistent with the illustrations of figures 3 and 7 of the Application; figure 2 shows that the 32-bit DATA output terminals are physically located at the left-hand side of the INTERFACE unit and the 32-DATA output signals are physically located at the right-hand side of the INTERFACE unit, and there is a one-to-one correspondence between the two groups of 32-bit DATA signals].

As to claim 5, Yanagawa teaches that **the value of p is one** [figure 3 shows a plurality of delay circuits; figures 8-11; figure 15; figure 25; p=1 as a delay circuit is associated with each strobe signal; a data acquisition circuit which delays the strobe signal (abstract); paragraph 0025.

As to claim 7, Yanagawa teaches that **the memory controller of claim 1, further including:**

a plurality of data input terminals that receive input data from the semiconductor memory device [figure 2, 32 bits DATA signals from the memory device (11)];

a signal input terminal [the STROBE SIGNAL shown in figure 2 between the memory device (11) and the interface unit (24)] **for every "q" data input terminals** [q=32 as shown in figure 2], **where "q" is an integer greater than 2** [q=32 as shown in figure 2], **each signal input terminal receiving an device input clock signal from the semiconductor memory device in synchronism with the input data** [figure 12 shows the CLK signal];

an input delay circuit corresponding to each signal input terminal that delays a received device input clock form the semiconductor memory device signal by a predetermined amount to generate an input strobe signal [figure 15; a data acquisition circuit which delays the strobe signal (abstract); paragraph 0025], **the input delay circuits being arranged between the signal input terminals and positions where the input delay circuits output the input strobe signals** [figures 2, 15]; **and an input holding circuit corresponding to each data input terminal** [data latch circuit, figure 15, 323], **each group of q input holding circuits holding input data in**

synchronism with the input strobe signal from a corresponding input delay circuit [figure 15]; **wherein the input data is transmitted to the data generating circuit through the data input terminals** [figure 2].

As to claim 8, Yanagawa teaches that **the memory controller of claim 1, further including:**

a plurality of data input terminals that receive input data from the semiconductor memory device [figure 2, 32 bits DATA signals from the memory device (11)];

a signal input terminal [the STROBE SIGNAL shown in figure 2 between the memory device (11) and the interface unit (24)] **for every "q" data input terminals** [q=32 as shown in figure 2], **where "q" is an integer greater than 2** [q=32 as shown in figure 2], **each signal input terminal receiving an device input clock signal from the semiconductor memory device in synchronism with the input data** [figure 12 shows the CLK signal];

an input delay circuit corresponding to each signal input terminal that delays a received device input clock form the semiconductor memory device signal by a predetermined amount to generate an input strobe signal [figure 15; a data acquisition circuit which delays the strobe signal (abstract); paragraph 0025], **the input delay circuits being arranged between the signal input terminals and positions where the input delay circuits output the input strobe signals** [figures 2, 15]; **and an input holding circuit corresponding to each data input terminal** [data latch circuit, figure 15, 323], **each group of q input holding circuits holding input data in synchronism with the input strobe signal from a corresponding input delay**

circuit [figure 15]; **wherein the input data is transmitted to the data generating circuit through the data input terminals** [figure 2];

a first wiring corresponding to each data input terminal that transmits digital data to a corresponding input holding circuit [figure 2 shows the wiring between 32 bits DATA and the latch circuit (27)]; **and**

a second wiring corresponding to each input holding circuit that transmits the input strobe signal from a corresponding input delay circuit to the input holding circuit [figure 2 shows the wiring to connect the STROBE signal to the delay circuit (26) then to the latch circuit (27)];

wherein the first and second wiring corresponding to each input holding circuit being essentially equal in length [paragraphs 0061-0064; refer to “Response to remark on claims 8 and 14”].

As to claim 9, Yanagawa teaches that **the m data output terminals are also data input terminals that receive input data from the semiconductor memory device in parallel** [figure 2 shows the 32 bits bidirectional DATA bus between the memory device and the memory controller]; **and**

the n signal output terminals are also signal input terminals for receiving device input clock signals from the semiconductor memory device in synchronism with the input data [figure 2 shows the STROBE SIGNAL as well as the CLK].

As to claim 10, Yanagawa teaches that **the output holding circuits transmit output digital data synchronously with both a rising edge and a falling edge of the output clock signal** [paragraph 0004].

As to claim 11, Yanagawa teaches that **the memory controller of claim 1, further including:**

a plurality of data input terminals that receive input data from the semiconductor memory device [figure 2, 32 bits DATA signals from the memory device (11)];

a signal input terminal [the STROBE SIGNAL shown in figure 2 between the memory device (11) and the interface unit (24)] **for every "q" data input terminals** [q=32 as shown in figure 2], **where "q" is an integer greater than 2** [q=32 as shown in figure 2], **each signal input terminal receiving an device input clock signal from the semiconductor memory device in synchronism with the input data** [figure 12 shows the CLK signal];

an input delay circuit corresponding to each signal input terminal that delays a received device input clock form the semiconductor memory device signal by a predetermined amount to generate an input strobe signal [figure 15; a data acquisition circuit which delays the strobe signal (abstract); paragraph 0025], **the input delay circuits being arranged between the signal input terminals and positions where the input delay circuits output the input strobe signals** [figures 2, 15]; **and an input holding circuit corresponding to each data input terminal** [data latch circuit, figure 15, 323], **each group of q input holding circuits holding input data in synchronism with the input strobe signal from a corresponding input delay circuit** [figure 15]; **wherein the input data is transmitted to the data generating circuit through the data input terminals** [figure 2];

wherein the input holding circuits transmit input data to the data generating circuit synchronously with both a rising edge and a falling edge of the corresponding input strobe signal [paragraph 0004].

As to claim 12, Yanagawa teaches that **the semiconductor memory device being coupled to the memory controller by the m data output terminals and the n signal output terminals** [figure 2].

As to claim 13, Yanagawa teaches that **the memory controller of claim 1, further including: a circuit core region** [figure 2, 10] **in which the clock generating circuit** [figure 2, 21)] **and data generating circuit are formed** [figure 2, 64bits→32bits and 32bits → 64bits]; **and**

an interface region [INTERFACE, figure 2, 24 and 25] **surrounding the circuit core region** [figure 2, 10] **in which the data output terminals** [DATA 32 bits, figure 2], **output holding circuits** [latch circuits (figure 2, 30 and 31)], **signal output terminals** [figure 2, STROBE SIGNAL], **and output delay circuits are formed** [DEALY CIRCUIT, figure 2, 26];

wherein each output holding circuit [figure 2, 64bits→32bits and 32bits → 64bits] **comprising a first latch circuit** [latch circuits (figure 2, 27, 30-33)].

As to claim 14, Yanagawa teaches that **the data output terminals are data input/output (I/O) terminals** [figure 2, 32bits DATA];

the signal output terminals are signal I/O terminals [figure 2, STROBE SIGNAL];

m input holding circuits corresponding to the data I/O terminals formed in the interface region [figure 2, 50], **each input holding circuit comprising a second**

latch circuit [the second latch circuit in figure 2, 27; the other latch circuits in figure 2, 30-33] **connected to a corresponding data I/O terminal by a first wiring** [figure 2, the wiring from 32 bits DATA to the latch circuit (27)], **the input holding circuits holding input data in synchronism with a corresponding input strobe signal** [figure 2, the STROBE signal leading to the delay circuit (26)]; **and**
an input delay circuit connected to each signal I/O terminal by a second wiring [figure 2, the wiring from the STROBE signal leading to the delay circuit (26)], **each input delay circuit delaying a received device input clock** [figure 2, the CLK signal leading to the holding circuit (50)] **from the semiconductor memory device signal by a predetermined amount to generate an input strobe signal** [figure 2, the STROBE signal leading to the delay circuit (26)], **each input strobe signal being connected to a corresponding second latch circuit by a third wiring** [figure 2, the wiring between the delay circuit (26) and the latch circuit (27)];
wherein the length of the first wiring to each second latch circuit is essentially equal to the sum of the lengths of the second and third wirings corresponding to the same second latch circuit [paragraphs 0061-0064; refer to "Response to remark on claims 8 and 14"].

As to claim 15, refer to "As to claim 1" and "As to claim 14."

As to claim 16, Yanagawa teaches that **the input delay circuits are arranged between the signal input terminals and locations where the input delay circuits output the input strobe signals** [figure 2, 50].

As to claim 17, refer to "As to claim 10."

As to claim 18, refer to "As to claim 12."

As to claim 19, refer to "As to claim 13."

As to claim 20, refer to "As to claim 2."

As to claim 21, refer to "As to claim 1" and "As to claim 7."

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3-4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagawa (US Patent Application Publication 2001/0046163), and in view of Kuge (US Patent Application Publication 2001/0014922).

Regading claims 3-4 and 6, Yanagawa does not teach the case where the value of p is greater than one, the case where the value of p is two, or the case where the value of p is selected from the group consisting one and two.

However, Kuge teaches in the invention "Interface Circuit Device for Performing Data Sampling at Optimum Strobe Timing" a method and apparatus of generating strobe signals using delay to obtain optimum sampling timing for data acquisition (abstract; figures 26, 36, 52). In particular, the scheme provides a strobe generation circuit for every 4 data terminals (figure 26). In addition, Kuge teaches that the association of the strobe timing circuit and the output terminals may be made on a byte

by byte basis, or be divided into a plurality of sets of bits, including the case where the set of bits is 2 (paragraphs 0198-0202).

Allocating the timing adjustment circuit for generating strobe based on more than one output terminal provides a flexible compromise between the cost of the system and the capability to fine-tuning the effective wiring length of each of the data line.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicant's invention to recognize the benefits of allocating the timing adjustment circuit for generating strobe based on more than one output terminal, as demonstrated by Kuge, and to incorporate it into the existing apparatus and method disclosed by Yanagawa, to further enhance the system's capability of fine-tuning the effective wiring length of each of the data line and provides better timing synchronization for data transfer.

7. ***Related Prior Art***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Zumkehr, (US Patent Application Publication 2003/0005346), "System and Method for Delaying a Strobe Signal."
- Noda et al., (US Patent Application Publication 2001/0015666), "Semiconductor Integrated Circuit Device, Semiconductor memory System and Clock Synchronous Circuit."

Conclusion

8. Claims 1-21 are rejected as explained above.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PIERRE BATAILLE
PRIMARY EXAMINER
2/1/06

PIERRE BATAILLE
PRIMARY EXAMINER